Amendments to the Specification

Please replace the title at page 1, line 1, with the following amended title:

METHOD AND SYSTEM FOR DYNAMICALLY ~~INCREASING OUTPUT RATE AND~~ REDUCING LENGTH OF A DELAY CHAIN

Please replace the paragraph at page 5, lines 6 through 12 with the following amended paragraph:

The design of the delay chain is illustrated in Fig. 2. As shown, the delay chain comprises 160 pipelined registers (~~reg1 – reg160~~en1 - en160) with the output of one register entering the next one. Since the clock rate and data rate are not the same, incoming and outgoing samples need to be qualified with a 'valid' signal. Each register has an enable logic (reg1 - reg160) that decides whether or not the register should be loaded with a new value. This logic is determined by the incoming valid signal and the SLOW/FAST mode in which the samples are being shifted out.